IN THE CLAIMS:

Claim 1. Canceled.

2. (Previously Presented) A processing apparatus comprising:

a memory capable of storing data;

a butterfly arithmetic unit for performing butterfly computation processes; and

a bit-reversed order shuffle processing unit for writing results obtained by the butterfly computation processes performed by said butterfly arithmetic unit at addresses in said memory after bit-reversed order shuffle instead of writing the results at addresses in said memory in processing order,

wherein data written by said bit-reversed order shuffle processing unit are discrete fast Fourier transform results and wherein

said processing apparatus further comprises

a complex conjugate data transforming unit for transforming input real data into complex data, and

an output reconstruction arithmetic unit for reading out the data written in said memory by said bit-reversed order shuffle processing unit and performing an output reconstruction computation process, wherein

said butterfly arithmetic unit performs a butterfly computation process for the complex conjugate data, and

output reconstruction computation process results obtained by said output reconstruction arithmetic unit are real discrete Fourier transform results.

3. (Previously Presented) A processing apparatus comprising:

a memory capable of storing data;

a butterfly arithmetic unit for performing butterfly computation processes; and

a bit-reversed order shuffle processing unit for writing results obtained by the butterfly computation processes performed by said butterfly arithmetic unit at addresses in said memory after bit-reversed order shuffle instead of writing the results at addresses in said memory in processing order,

wherein data written by said bit-reversed order shuffle processing unit are discrete fast Fourier transform results and wherein

said processing apparatus further comprises an output reconstruction arithmetic unit for performing an output reconstruction computation process, wherein

said butterfly arithmetic unit performs a butterfly computation process for the data having undergone the output reconstruction computation process, and

the data written by said bit-reversed order shuffle processing unit are real inverse discrete Fourier transform results.

4. (Previously Presented) A processing apparatus comprising:

a memory capable of storing data;

a butterfly arithmetic unit for performing butterfly computation processes; and

a bit-reversed order shuffle processing unit for writing results obtained by the butterfly computation processes performed by said butterfly arithmetic unit at addresses in said memory after bit-reversed order shuffle instead of writing the results at addresses in said memory in processing order,

wherein data written by said bit-reversed order shuffle processing unit are discrete fast Fourier transform results and wherein

said butterfly arithmetic unit reads out data from said memory and performs a butterfly computation process, and

said bit-reversed order shuffle processing unit leaves necessary data to be read out from said memory by said butterfly arithmetic unit afterward and overwrites the butterfly computation process results at addresses of unnecessary data that have already been read out.

5. (Original) The processing apparatus according to claim 4, wherein said butterfly arithmetic unit controls a read sequence of data from said memory so as to prevent said bit-reversed order shuffle processing unit from overwriting the necessary data.

Claim 6. Canceled.

7. (Previously Presented) A processing apparatus comprising:

a butterfly arithmetic unit for performing butterfly computation processes and writing results obtained by the butterfly computation processes in a memory; and

a bit-reversed order shuffle processing unit for reading out the results obtained by the butterfly computation processes and written in the memory from addresses in the memory upon bit-reversed order shuffle,

wherein data read out by said bit-reversed order shuffle processing unit are discrete fast Fourier transform results and wherein

said processing apparatus further comprises

a complex conjugate data transforming unit for transforming input real data into complex data, and

an output reconstruction arithmetic unit for performing an output reconstruction computation process for the data read out by said bit-reversed order shuffle processing unit, wherein

said butterfly arithmetic unit performs a butterfly computation process for the complex conjugate data, and

output reconstruction computation process results obtained by said output reconstruction arithmetic unit are real discrete Fourier transform results.

8. (Previously Presented) A processing apparatus comprising:

a butterfly arithmetic unit for performing butterfly computation processes and writing results obtained by the butterfly computation processes in a memory; and

a bit-reversed order shuffle processing unit for reading out the results obtained by the butterfly computation processes and written in the memory from addresses in the memory upon bit-reversed order shuffle,

wherein data read out by said bit-reversed order shuffle processing unit are discrete fast Fourier transform results and wherein

said processing apparatus further comprises an output reconstruction arithmetic unit for performing an output reconstruction computation process, wherein

said butterfly arithmetic unit performs a butterfly computation process for the data having undergone the output reconstruction computation process, and

the data read out by said bit-reversed order shuffle processing unit are real inverse discrete Fourier transform results.

9. (Previously Presented) A processing apparatus comprising:

a butterfly arithmetic unit for performing butterfly computation processes and writing results obtained by the butterfly computation processes in a memory;

a bit-reversed order shuffle processing unit for reading out the results obtained by the butterfly computation processes and written in the memory from addresses in the memory upon bit-reversed order shuffle; and

a post-processing unit for processing the data read out by said bit-reversed order shuffle processing unit,

wherein data read out by said bit-reversed order shuffle processing unit are discrete fast Fourier transform results.

10. (Original) The processing apparatus according to claim 9, wherein said post-processing unit leaves necessary data to be read out from said memory by said bit-reversed order shuffle processing unit afterward and overwrites process results at addresses of unnecessary data that have already been read out.

11. (Original) The processing apparatus according to 10, wherein said bit-reversed order shuffle processing unit controls a read sequence of data from said memory so as to prevent said post-processing unit from overwriting the necessary data.

12. (Previously Presented) A processing apparatus for executing a sequence of reading out data one by one from an external unit or a memory, performing a series of computation processes including a discrete fast Fourier transform process for the data, and writing the data in the memory, as one unit, with respect to all the data sequentially and repeatedly under pipeline sequence control adjusted to inhibit concurrent execution of computations of the same type, thereby processing one computation process group, and deriving computation results by continuously executing the series of computation processes, comprising:

an arithmetic unit for executing a computation of input data; and

a memory for storing a computation result obtained by said arithmetic unit,

wherein said arithmetic unit has a process latency until the input data is input and processed and the process result is output, the process latency being a time adjusted to inhibit data in the memory which is required for a subsequent computation process during a computation process from being overwritten by output data, and

a bit-reversed order shuffle process group and an immediately preceding or succeeding process group are processed in a sequence as one unit by said arithmetic unit having the process latency.

13. (Previously Presented) The processing apparatus according to claim 12, wherein a bit-reversed order shuffle process group of a discrete fast Fourier transform process and an immediately preceding butterfly computation process group are processed in a sequence as one unit.

14. (Original) The processing apparatus according to claim 13, wherein a real discrete Fourier transform is performed.

15. (Original) The processing apparatus according to claim 13, wherein a real inverse discrete Fourier transform is performed.

16. (Currently Amended) The processing apparatus according to claim 12, wherein a bit-reversed order shuffle process group of a real discrete Fourier transform process and an immediately succeeding output reconstruction computation process group are processed in a sequence as one unit.

Claims 17-20. Cancelled

21. (Previously Presented) A processing method comprising:

providing a memory capable of storing data;

transforming input real data into complex data;

performing butterfly computation processes for the complex conjugate data;

bit-reversed order shuffle processing the results obtained by the butterfly computation process to obtain discrete fast Fourier transform results;

writing the discrete fast Fourier transform results at addresses in the memory instead of writing the results of the butterfly computation processes at addresses in the memory in processing order;

reading out the discrete fast Fourier transform data written in the memory; and

output reconstruction computation processing the discrete fast Fourier transform data read from the memory to obtain real discrete fast Fourier transform results.

22. (Previously Presented) A processing method comprising:

providing a memory capable of storing data;

performing an output reconstruction computation process;

butterfly computation processing data having undergone the output reconstruction computation process;

bit-reversed order shuffle processing the results obtained by the butterfly computation process to obtain real inverse discrete fast Fourier transform results; and

writing the real inverse discrete Fourier transform results at addresses in the memory instead of writing the results of the butterfly computation processes at addresses in the memory in processing order.

23. (Previously Presented) A processing method comprising:

providing a memory capable of storing data;

reading data from the memory;

butterfly computation processing the data read from the memory;

bit-reversed order shuffle processing the results obtained by the butterfly computation process to obtain discrete fast Fourier transform results; and

writing the discrete fast Fourier transform results at addresses of unnecessary data in the memory instead of writing the results of the butterfly computation processes at addresses in the memory in processing order, the addresses of unnecessary data are addresses for data that has been already been read out and butterfly computation processed, wherein necessary data for the butterfly computation processing is not overwritten.

24. (Previously Presented) A processing method comprising:

transforming input real data into complex data

butterfly computation processing the complex conjugate data and writing results obtained by the butterfly computation processes in a memory;

reading the results from the memory using a bit-reversed order shuffle process to obtain discrete fast Fourier transform results; and

performing an output reconstruction computation process on the discrete fast Fourier transform results to obtain real discrete fast Fourier transform results.

25. (Previously Presented) A processing method comprising:

performing an output reconstruction computation process;

butterfly computation processing data having undergone the output reconstruction computation process;

writing results obtained by the butterfly computation processes in a memory; and

reading out the results obtained by the butterfly computation processes and written in the memory from addresses in the memory using a bit-reversed order shuffle process to obtain real inverse discrete fast Fourier transform results.

26. (Currently Amended) A processing method comprising:

performing butterfly computation processes and writing results obtained by the butterfly computation processes in a memory;

reading out the results obtained by the butterfly computation processes and written in the memory from addresses in the memory ~~using a~~ upon bit-reversed order shuffle ~~process to obtain discrete fast Fourier transform results~~; and

~~post~~ processing the data read out in said bit-reversed order shuffle, wherein said data read out in said bit-reversed order shuffle are discrete fast Fourier transform results.

27-32. (Canceled)